APPENDIX A

"CLEAN" VERSION OF EACH PARAGRAPH/SECTION/CLAIM

37 C.F.R. § 1.121(b)(ii) AND (c)(i)

CLAIMS (with indication of amended or new):

(AMENDED) 34. The device of claim 29, wherein:

at least a plurality of said active trenches containing MOS gated structures are polygonal in topology and are symmetrically spaced and disposed over the surface of said silicon wafer;

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said source regions surrounding respective ones of said active trenches containing a MOS gated structure;

said intermediate trenches surrounding said at least a plurality of said active trenches consisting of a trench of lattice shape in topology which extends in the space defined between spaced active trenches having said polygonal topology.

(AMENDED) 41. A trench MOS gated device which has improved resistance to both high radiation and single event high energy charged particles (SEE), comprising:

a silicon wafer of one conductivity type having a plurality of spaced shallow active trenches containing respective gate structures and a plurality of intermediate trenches each disposed between a respective pair of active trenches;

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each of said active trenches and each of said intermediate trenches having at least partly vertical walls joined at their bottoms by respective trench bottoms;

each of said active trenches containing a gate structure having a gate dielectric on at least portions of its said vertical walls, a bottom dielectric on the bottom and a conductive polysilicon plug of said one conductivity type which acts as a gate electrode and which contacts at least the interior surface of said gate dielectric;

each of said intermediate trenches having a shallow diffusion of a conductivity type opposite to said one conductivity type extending from its walls and bottom and being filled with a conductive polysilicon plug of said opposite conductivity type;

the spaces between said active and intermediate trenches each containing a channel region of said opposite conductivity type and an upper source region comprising a diffusion in contact with said respective polysilicon plugs in said corresponding intermediate trenches;

a common source contact contacting each of said source regions and each of said conductive plugs in each of said intermediate trenches; and

a common gate electrode connected to each of said conductive plugs in each of said active trenches containing a gate structure and a drain contact connected to a drift region beneath said active and intermediate trenches;

wherein the thickness of said gate dielectric is chosen to optimize resistance to high radiation effects and wherein the thickness of said bottom dielectric is chosen to optimize resistance to SEE; and

wherein said trench MOS gated device is supported in a die which further contains a termination structure; said plurality of active trenches and said plurality of intermediate trenches defining an active area; said termination structure comprising a plurality of concentric ring-shaped trenches surrounding said active area and extending radially from said active area toward the edge of said die; each of said plurality of ring-shaped trenches having a diffusion extending from its walls and bottom which is of said opposite conductivity type; each of said plurality of ring-shaped trenches having a conductive polysilicon plug of said opposite conductivity type; said plurality of ring-shaped trenches being out of direct contact with said source contact and comprising floating rings.

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(AMENDED) 42. A trench MOS gated device which has improved resistance to both high radiation and single event high energy charged particles (SEE), comprising:

a silicon wafer of one conductivity type having a plurality of spaced shallow active trenches containing respective gate structures and a plurality of intermediate trenches each disposed between a respective pair of active trenches;

each of said active trenches and each of said intermediate trenches having at least partly vertical walls joined at their bottoms by respective trench bottoms;

each of said active trenches containing a gate structure having a gate dielectric on at least portions of its said vertical walls, a bottom dielectric on the bottom and a conductive polysilicon

plug of said one conductivity type which acts as a gate electrode and which contacts at least the interior surface of said gate dielectric;

each of said intermediate trenches having a shallow diffusion of a conductivity type opposite to said one conductivity type extending from its walls and bottom and being filled with a conductive polysilicon plug of said opposite conductivity type;

the spaces between said active and intermediate trenches each containing a channel region of said opposite conductivity type and an upper source region comprising a diffusion in contact with said respective polysilicon plugs in said corresponding intermediate trenches;

a common source contact contacting each of said source regions and each of said conductive plugs in each of said intermediate trenches; and

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a common gate electrode connected to each of said conductive plugs in each of said active trenches containing a gate structure and a drain contact connected to a drift region beneath said active and intermediate trenches;

wherein said trench MOS gated device is supported in a die which further contains a termination structure; said plurality of active trenches containing a gate structure and said plurality of intermediate trenches defining an active area; said termination structure comprising a plurality of concentric ring-shaped trenches surrounding said active area and extending radially from said active area toward the edge of said die; each of said plurality of ring-shaped trenches having a diffusion extending from its walls and bottom which is of said opposite conductivity type; each of said plurality of ring-shaped trenches having a conductive polysilicon plug of said opposite conductivity type; said plurality of ring-shaped trenches being out of direct contact with said source contact and comprising floating rings.

(NEW) 45. The device of claim 36, wherein said trench MOS gated device is supported in a die which further contains a termination structure; said plurality of active trenches and said plurality of intermediate trenches defining an active area; said termination structure comprising at least a ring-shaped trench surrounding said active area and extending from said active area toward the edge of said die; said ring-shaped trench having a diffusion extending from its walls and bottom which is of said opposite conductivity type; said ring-shaped trench

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having a conductive polysilicon plug of said opposite conductivity type; said ring-shaped trench being out of direct contact with said source contact and comprising a floating ring.

(NEW) 46. The device of claim 29, wherein said trench MOS gated device is supported in a die which further contains a termination structure; said plurality of active trenches and said plurality of intermediate trenches defining an active area; said termination structure comprising at least a ring-shaped trench surrounding said active area and extending from said active area toward the edge of said die; said ring-shaped trench having a diffusion extending from its walls and bottom which is of said opposite conductivity type; said ring-shaped trench having a conductive polysilicon plug of said opposite conductivity type; said ring-shaped trench being out of direct contact with said source contact and comprising a floating ring.